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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/620,679	07/20/2000	Rodney Ruesch	499.075US1	3177
759	90 03/14/2002			
Schwegman, Lundberg, Woessner & Kluth, P.A.			EXAMINER	
P.O. Box 2938 Minneapolis, MN 55402			LE, DON P	
			ART UNIT	PAPER NUMBER
		2819		
			DATE MAILED: 03/14/2002	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary Examin r	•		Application No.	Applicant(s)			
Examin r Don P Le 2819	Office Action Summary						
Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MULLING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILLING DATE OF THIS COMMUNICATION. Educations of time range the available under the previous or 37 CFR 1.38(a). In no event, however, may a reply be timely filled under 35 (b) MONTHS from the maining date of this communication. If the period for reply specified above is lies about hidy (20) days, a reply within the stat or exemption and the state of the communication of the 37 CFR 1.38(a). In no event, however, may a reply be timely filled under 35 (b) MONTHS from the mailing date of this communication. If the period for reply specified above is lies about hidy (20) days, a reply within the stat or exemption and provide a replication. Failur for reply within the stat or excended period for regive they are unaison. Failur for reply within the stat or excended period for regive they are unaison. Failur for reply within the stat or excended period for regive they are unaison. Part of the communication of the mailing date of this communication, even if timely filed, may reduce any summed patient and adjustment. Status Responsive to communication(s) filed on 30 January 2002. 2a) This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4) Claim(s) 1.25 is/are pending in the application. 4a) Of the above claim(s) 1.6 and 17-22 is/are withdrawn from consideration. 5) Claim(s) 1.14 is/are objected to by the Examiner. Application Papers 9) The specification is objected to by the Examiner. Application Papers 9) The proposed drawing correction filed on							
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THE MAILING DATE OF THIS COMMUNICATION. Extensions or time may be existed with early the provision of 30 CPR 1.13(e). In no event, however, may a neply be timely filled effect \$X. (6) MONTHS from the mailing date of this communication. If the period on party specified size is best him thin (20) days, a regive with the station or interpretation of the provision of 10 CPR 1.13(e). Failure to reply within the set or extended period for reply with, by statute, cause the application to become ABANDONED (35 U.S. C. § 133). Failure to reply within the set or extended period for reply with, by statute, cause the application to become ABANDONED (35 U.S. C. § 133). Any reply received by the Office time then three months failtre the mailing date of this communication, even if timely filled, may reduce any example under turn education in the provision of the communication of the communication. Set of this communication, even if timely filled, may reduce any example under turn education is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Exparte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Exparte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4) Claim(s) 1-25 is/are pending in the application. 4a) Of the above claim(s) 1-6 and 17-22 is/are withdrawn from consideration. 5) Claim(s) 1-14 is/are objected to. 5) Claim(s) 1-15 is and 23-25 is/are rejected. 7) Claim(s) 1-15 is and 23-25 is/are rejected. 7) Claim(s) 1-15 is and 23-25 is/are rejected. 7) The proposed drawing correction filed on is/are: a) accepted or b) by the Examiner. 10) The drawing(s) filed on is/are: a) accepted or b) disapproved by the Examiner. If approved, corrected drawings are required in reply to this Office action. 12) The proposed drawing correction filed on is: a) accepte							
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Application/Control Number: 09/620,679 Page 2

Art Unit: 2819

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.
- 2. Claims 7 and 23-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Knee et al. (US 5,337,254).
- 3. With respect to claim 7, figures 1-4 of Knee teaches a method of communicating data in an integrated circuit using internal interconnects, the method comprising:

receiving a data signal (100);

adjusting a first resistance (activating transistor 1X connected to VDD at 110, figure 3) coupled to a first supply voltage (VDD), based on a manufacturing process, the first supply voltage and a temperature (PVT control signal from 18 through microprocessor to 70, figure 1);

adjusting a second resistance (activating another transistor 1X connected to ground at 110, figure 3) coupled to a second supply voltage (ground), based on the

Page 3

Art Unit: 2819

manufacturing process, the first supply voltage and the temperature (PVT control signal from 18 through microprocessor to 70); and

adjusting a third resistance (activating another transistor 2X connected to ground at 112, figure 1) coupled to the second supply voltage (ground), based on the manufacturing process, the first supply voltage and a temperature (PVT control signal from 18 through microprocessor to 72).

- 4. With respect to claim 23, figure 3 of Knee teaches adjusting a first resistance (1X of 110) includes changing a resistance of a semiconductor.
- 5. With respect to claim 24, figure 3 of Knee teaches adjusting a first resistance includes changing a gate voltage on a field effect transistor (FET).
- 6. With respect to claim 25, figure 1 of Knee teaches selecting a predetermined number of programmable bits from a plurality of programmable bits (microprocessor provides bits (inputs to 70, 72, 74) to 16 to control the resistance.)
- 7. Claims 8-10, 15, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Esch, Jr. (US 6,118,310).
- 8. With respect to claim 8, figures 4-6 of Esch teaches a method of communicating data in an integrated circuit using internal interconnections, the method comprising:

selecting a resistance of a divider network (select resistor based on 262, 264 of figure 6) based on a manufacturing process, a supply voltage and a temperature;

Art Unit: 2819

selecting an edge rate of a driver (edge rate is controlled by 266) coupled to the divider network, the selected edge rate based on the manufacturing process, the supply voltage and the temperature;

Page 4

receiving a data signal (203); and

providing an output (output at 241) based on the data signal, the resistance, and the edge rate.

- 9. With respect to claim 9, figure 6 of Esch teaches selecting an edge rate of a driver coupled to the divider network comprises maintaining a substantially constant edge rate.
- 10. With respect to claim 10, figure 5 of Esch teaches providing an output turning on a PFET transistor (212) and turning off an NFET transistor (222).
- 11. With respect to claim 15, figure 5 of Esch discloses the step of receiving a tristate enable signal (ENABLE); and actuating a switchable resistance element (230) in response to the tristate enable signal.
- 12. With respect to claim 16, figure 5 of Esch discloses actuating a switchable resistance element comprises actuating a programmable inverter (230 configured as inverter).

Allowable Subject Matter

13. Claims 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Application/Control Number: 09/620,679 Page 5

Art Unit: 2819

14. The following is an examiner's statement of reasons for allowance:

With respect to claim 11, in addition to other elements inn the claim, the prior art does not teach a method of communicating data having a step of selecting a resistance of a divider network comprises selecting a plurality of parallel resistance elements.

With respect to claim 12, in addition to other elements inn the claim, the prior art does not teach a method of communicating data having a step of selecting a resistance of a divider network comprises executing programming for selecting resistance elements from a plurality of switchable resistance elements.

With respect to claim 11, in addition to other elements inn the claim, the prior art does not teach a method of communicating data having a step of selecting an edge rate of a driver coupled to a divider network comprises programming for selecting resistance elements from a parallel resistance elements.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

14. Applicant's arguments filed 1/30/2002 have been fully considered but they are not persuasive.

Application/Control Number: 09/620,679 Page 6

Art Unit: 2819

With respect to claim 7, applicant arguments that the prior art "Knee does not discuss concerning adjusting resistance," the apparatus of Knee has the option of adjusting the output resistance of the I/O circuit (figure 3), by activating certain pull-up or pull-down transistors (1X-4X). Therefore, the claim element is anticipated.

With respect to claim 7, applicant argues that the term "ground" does not meet the second supply voltage of the claim. The claim does not specify the second supply voltage to be at a certain potential. Ground voltage is considered to be at a certain potential. Therefore, ground supply voltage is broadly interpreted as a second supply. Therefore, the claimed element is anticipated.

With respect to claim 24, applicant argues that the prior art does not teach changing a gate voltage on a field effect transistor. Figure 3 of Knee discloses the transistors (1X-4X) are activated buying changing the gate voltage (low or high logic level). Therefore, the claim element is anticipated.

With respect to claim 25, applicant argues that Knee does not teach "selecting a predetermined number of programmable bits from a plurality of bits". Figures 1 and 3 of Knee shows the microprocessor providing controlling bits to 70, 72 and 74 to activate particular transistors 1X-4X. Therefore, the claim element is anticipated.

With respect to claim 8, applicant argues that figure 6 of Esch does not teach, "selecting a resistance of a divider network based on a manufacturing process, a

Art Unit: 2819

supply voltage and a temperature." Figure 6 of Esch show a divider network comprising 262 and 264, and a resistance based on the divider network is applied to 260 based on the PVT of the semiconductor (see column 5, lines 5-15).

With respect to claim 8, applicant argues that there is no discussion concerning edge rate in the apparatus of Esch. Applicant is correct in that Esch does not specifically written anywhere in the specification concerning edge rate. This feature is inherent in the apparatus of Esch as shown in figure 4, by activating certain transistors (211..229), the edge rate of the driver depends on which transistors are activated. Therefore, the claim element is anticipated.

With respect to claim 9, applicant argues that Esch does not teach maintaining a substantially constant edge rate. Esch does not show "word for word" of maintaining a substantially constant edge rate as claimed by applicant.

However, Esch teaches maintaining a constant output impedance over a wide range of PVT conditions (see column 2, lines 10-20 and column 4, lines 35-40).

Particularly, Esch's invention provides constant voltage output by varying output impedance. Therefore, the edge rate of the output signal is constant.

With respect to claim 15, applicant argues that Esch does not teach, "Receiving a tristate enable signal and actuating resistance element in response to the tristate enable signal." Figure 5 of Esch shows an enable signal (ENABLE) controlling a switchable resistance element 230. Therefore, the claimed element is anticipated.

Art Unit: 2819

With respect to claim 16, applicant argues that Esch does not teach actuating a programmable inverter. Figure 5 of Esch shows the output of the switching element 230 is an inverted output based on the enable signal. When the enable signal is high logic level, the output of 230 is low logic level and when the enable signal is low logic level the output of 230 is high logic level. Therefore, the switchable element is a programmable inverter.

16. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P Le whose telephone number is 703-308-4890. The examiner can normally be reached on 7AM - 5PM.

Art Unit: 2819

Final communications.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7724 for After

Page 9

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Don Phu le

March 12, 2002